Engineering Hardware Specification

of the

Atari ST Computer System

The Atari Corporation

Sunnyvale, California

7 January 1986

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   THE SCOPE OF THIS DOCUMENT is limited to a description
of the ST computer system hardware characteristics and
idiosyncrasies. This document does not provide a detailed
description of ST component parts, peripheral devices, dev-
ice protocols, or software. References are provided for
detailed inquiry.

1. System Architecture

```
      -----------                      -----------
     |Graphics   |                    |Music      |
     |Subsystem  |                    |Subsystem  |
      -----------                      -----------
           |                                |
           |         -----------            |
      --------------| Main      |--------
                    | System    |
                     -----------
                          |
                          |              -----------
     The ST                    --------|Device     |
                                       |Subsystems |
                                        -----------
```
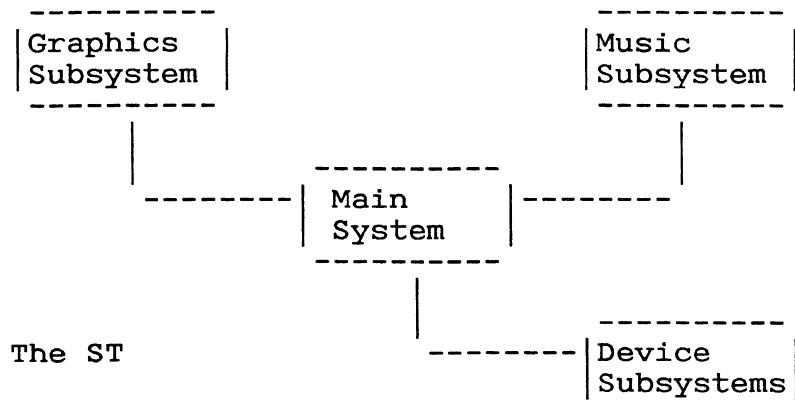
   The hardware architecture of the Atari Corporation ST
(Sixteen/Thirty-two) computer system consists of a main sys-
tem, a graphics subsystem, a music subsystem, and several
device subsystems (most of the device subsystems require ST
resident intelligence). The ST is based on the MC68000 16
bit data/24 bit address microprocessor unit capable of
directly accessing up to 16 Mbytes of ROM and RAM memory.
Hardware features of the ST computer system include:

Main System
        o 16 bit data/24 bit address 8 MHz microprocessor unit
        o 192 Kbyte ROM, cartridge expandable to 320 Kbyte
        o 512 Kbyte RAM or 1 Mbyte RAM
        o direct memory access support

Graphics Subsystem
        o 32 Kbyte BitMap video display memory (from above)
        o 320 x 200 pixel, 16 color palette from 512 selections
        o 640 x 200 pixel, 4 color palette from 512 selections
        o 640 x 400 pixel, monochrome

Music Subsystem
        o programmable sound synthesizer
        o musical instrument network communication

Device Subsystems
       o   intelligent keyboard
   o   two button mouse
       o   RGB color and monochrome monitor interfaces
       o   printer parallel interface
       o   RS232 serial interface
       o   MIDI musical instrument interface
       o   on board floppy disk controller and DMA interface
       o   hard disk drive DMA interface

     The following is a simplified hardware system block
diagram of the Atari ST:

----- Atari ST System Block Diagram ---------------

```
----------------
| MC68000 MPU   |<--
----------------    |
                    |
                    |              ----------
       ------------ |      <------------------------->|192 Kbyte |<--->EXPAN
       ------------ |      ------------------------->| ROM      |
                  | |                                 ----------
                  | |                                 ----------
                  | |                                 |512K or 1M|
       ----------   |                         -->|  byte RAM |<--
       | Control  |<----->|<----->| Memory   |<--    ----------    |
       | Logic    |------->------->| Controller|<--                  |
       ----------   |       ----------                ----------       |
        | | | |  |  |                        -->| Video    |<-- RF MOD
        | | | |  |  |<----->| Buffers  |<----->| Shifter  |---->RGB
        | | | |  |  |       ----------          ----------     MONO
        | | | |  |  |       ----------          ----------
        | | | |  |  |<----->| MC6850   |<----->| Keyboard |<--->IKBD
        | | | ----------|------->| ACIA     |       | Port     |
        | | | |  |  |       ----------          ----------
        | | | |  |  |       ----------          ----------
        | | | |  |  |<----->| MC6850   |<----->| MIDI     |->OUT/THRU
        | | ----------------|------->| ACIA     |       | Ports    |<----IN
        | | |  |  |       ----------          ----------
        | | |  |  |       ----------          ----------
        | | |  |  |<----->| MK68901  |<----->| RS232    |<--->MODEM
        | ------------------|------->| MFP      |<--    | Port     |
        |   |  |  |       ----------    |      ----------
        |   |  |  |                     |      ----------
        |   |  |  |                  ---| Parallel |<->PRINTER
        |   |  |  |                  -->| Port     |
        |   |  |  |       ----------    |  ----------
        |   |  |  |<----->| YM-2149  |<--  ----------
        --------------------|------->| PSG      |------->| Sound    |---->AUDIO
            |  |  |       ----------  ---    | Channels |
            |  |  |       ----------    |  ----------
            |  |  |                     |  ----------
            |  |  |       ----------  -->| Floppy   |<->FLOPPY
            |  |  |<-------| WD1772   |<----->|Disk Port |    DRIVE
            |  |    -->| FDC      |       ----------
            |  |    |  ----------
            |  |    -->| DMA      |       ----------
            |  |<----->| Controller|<----->|Hard Disk |<--->HARD
            --------------------------->|           |       | Port     |    DRIVE
                        ----------          ----------
```

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2. Main System

```
 ----------                    ----------
|          |                  |          |
|          |                  |          |
 ----------     ----------     ----------
     |         |          |        |
      --------| Main      |--------
             | System     |
              ----------
                  |
                   --------|          |
                          |          |
                           ----------
```

The main system includes the microprocessor unit, main memory (both ROM and RAM), and general purpose DMA controller. The main system is limited to memory expansion only and should not be considered an open system (except via the high speed device interfaces).

2.1. Microprocessor Unit

The ST computer system is based on an 8 MHz MC68000 16 bit data/24 bit address microprocessor unit (with an internal 32 bit architecture). Some features of the MC68000 are: eight 32 bit data registers, nine 32 bit address registers, a 16 Mbyte direct addressing range, 14 addressing modes, memory mapped I/O, five data types, and a 56 instruction set. The MPU is directly supported by an MK68901 Multi Function Peripheral providing general purpose interrupt control and timers, among other things.

2.2. Memory Configuration

The configuration of main memory consists of five 64 Kbyte sets of ROM (standard set0 to set2, expansion set3 and set4) and one configurable bank (standard bank0) of 128 Kbyte, 512 Kbyte, or 2 Mbyte RAM. The configuration of main memory ROM is ascertained through software identification. The configuration of main memory RAM is achieved via the programming of the Memory Configuration Register (read/write, reset: all zeros). RAM configuration must be asserted during the first steps of the power up sequence and can be determined by using the following shadow test algorithm:

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```
START    o   write 0x000a (2 Mbyte, 2 Mbyte) to the Memory
             Configuration Register.

BANK0    o   write Pattern to 0x000000 - 0x0001ff.
         o   read Pattern from 0x000200 - 0x0003ff.
         o   if Match, then Bank0 contains 128 Kbyte; goto BANK1.
         o   read Pattern from 0x000400 - 0x0005ff.
         o   if Match, then Bank0 contains 512 Kbyte; goto BANK1.
         o   read Pattern from 0x000000 - 0x0001ff.
         o   if Match, then Bank0 contains 2 Mbyte; goto BANK1.
         o   panic:  RAM error in Bank0.

BANK1    o   write Pattern to 0x200000 - 0x2001ff.
         o   read Pattern from 0x200200 - 0x2003ff.
         o   if Match, then Bank1 contains 128 Kbyte; goto FIN.
         o   read Pattern from 0x200400 - 0x2005ff.
         o   if Match, then Bank1 contains 512 Kbyte; goto FIN.
         o   read Pattern from 0x200000 - 0x2001ff.
         o   if Match, then Bank1 contains 2 Mbyte; goto FIN.
         o   note:  Bank1 nonexistent.

FIN      o   write Configuration to the Memory Configuration
             Register.
         o   note Total Memory Size (Top of RAM) for future
             reference.
```

RAM memory access cycles are interleaved between the microprocessor unit and the video controller, thus allowing video display memory to reside efficiently as part of main memory (the MPU still maintains full memory bandwidth).

2.3. Direct Memory Access

A direct main memory RAM access channel is shared to provide support for both low speed (250 to 500 Kbits/sec) and high speed (up to 12 Mbits/sec) 8 bit device controllers. The base address for the DMA read or write operation is loaded into the DMA Base Address and Counter Register (read/write, reset: all zeros). Since only one counter register and channel is provided, only one DMA operation can be executed at a time.

The actual DMA operation is performed through a 32 byte FIFO programmed via the DMA Mode Control Register (word access write only, reset: not affected) and DMA Sector Count Register (word access write only, reset: all zeros). The progress, success, or failure of a DMA operation is reported through the DMA Status Register (word access read only, reset: one) which is cleared by toggling Write/_Read in the DMA Mode Control Register.

Bus accesses are granted to the DMA controller and MC68000 MPU on an egalitarian first come, first served basis. The access remains in effect until an operation is complete or until control is otherwise relinquished.

3. Graphics Subsystem

```
 ----------                          ----------
|Graphics  |                        |          |
|Subsystem |                        |          |
 ----------                          ----------
     |              ----------            |
      --------|          |--------
             |          |
              ----------
                  |
                   --------|          |
                          |          |
                           ----------
```
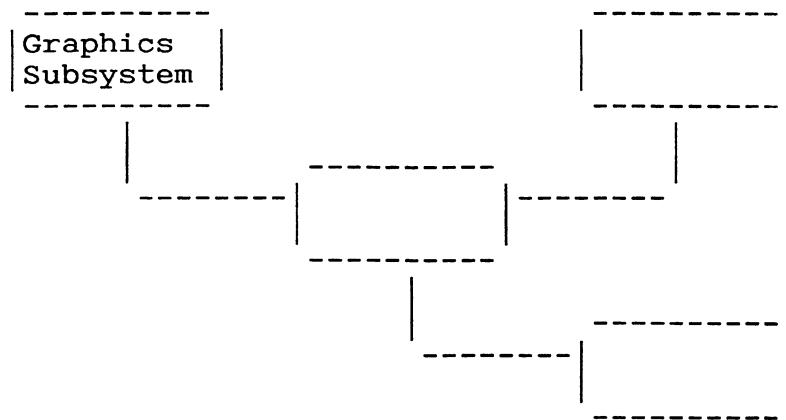
The basic components of the graphics subsystem are video display memory and the video controller. The definitions of BitMap, BitBlk, BitBlt, coordinate system, and color model are left to higher logical (software) levels of system specification.

3.1. Video Display Memory

Video display memory is configured as n logical planes interwoven by 16 bit words into contiguous memory to form one 32 Kbyte (actually 0x7d00) physical plane starting at any 256 byte half page boundary (in RAM only). The starting address of display memory is placed in the Video Base Address Register (read/write, reset: all zeros) which is then loaded into the Video Address Counter Register (read only, reset: all zeros) and incremented. The following is a diagram of possible physical configurations of video display memory:

```
                       --------
16 bit word           |        |
                       --------  -------- -------- -------- --------
4 plane               |plane 0 |plane 1 |plane 2 |plane 3 |plane 0 |
                       --------  -------- -------- -------- --------
2 plane               |plane 0 |plane 1 |plane 0 |plane 1 |plane 0 |
                       --------  -------- -------- -------- --------
1 plane               |plane 0 |plane 0 |plane 0 |plane 0 |plane 0 |
                       --------  -------- -------- -------- --------
```
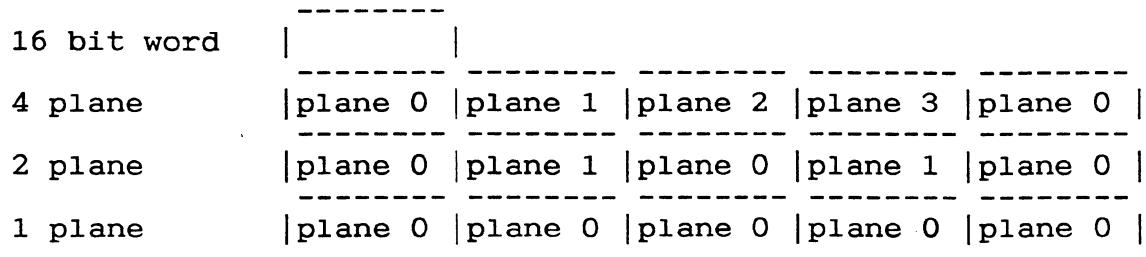
Display memory resides as part of main memory and has
an identical bit, byte, and word arrangement with the physi-
cal screen origin located at top left (bit 15):


```
                  high       low
                ---------  ---------
word 0          | byte 0 | byte 1 |
                ---------  ---------
                fedcba98 76543210
```


3.2. Video Configuration

The ST possesses three modes of video configuration:
320 x 200 resolution with 4 planes, 640 x 200 resolution
with 2 planes, and 640 x 400 resolution with 1 plane.   The
modes are set through the Shift Mode Register (read/write,
reset: all zeros). A sixteen word color lookup palette is
provided with nine bits of color per entry. The sixteen
Color Palette Registers (read/write, reset: not affected)
contain three bits of red, green, and blue aligned on low
nibble boundaries. Eight intensity levels of red, eight
intensity levels of green, and eight intensity levels of
blue produce a total of 512 possible colors.

In 320 x 200 4 plane mode all sixteen palette colors
can be indexed, while in 640 x 200 2 plane mode only the
first four palette entries are applicable.   In 640 x 400
monochrome mode the color palette is bypassed altogether and
is instead provided with an inverter for inverse video con-
trolled by bit 0 of palette color 0 (normal video is black
0, white 1). Color palette memory is arranged the same as
main memory.   Palette color 0 is also used to assign a
border color while in a multi-plane mode.   In monochrome
mode the border color is always black.

The general flow of the video controller is as follows:
BitMap planes are taken a word at a time from video display
memory and placed in the video shift register where one bit
from each plane is shifted out and collectively used as an
index (plane 0 is the least significant bit) to a color
lookup palette entry which is supplied to 3 bit digital to
analog converters to produce RGB output. The following is a
block diagram of the video controller:

----- Video Controller Block Diagram ---------------
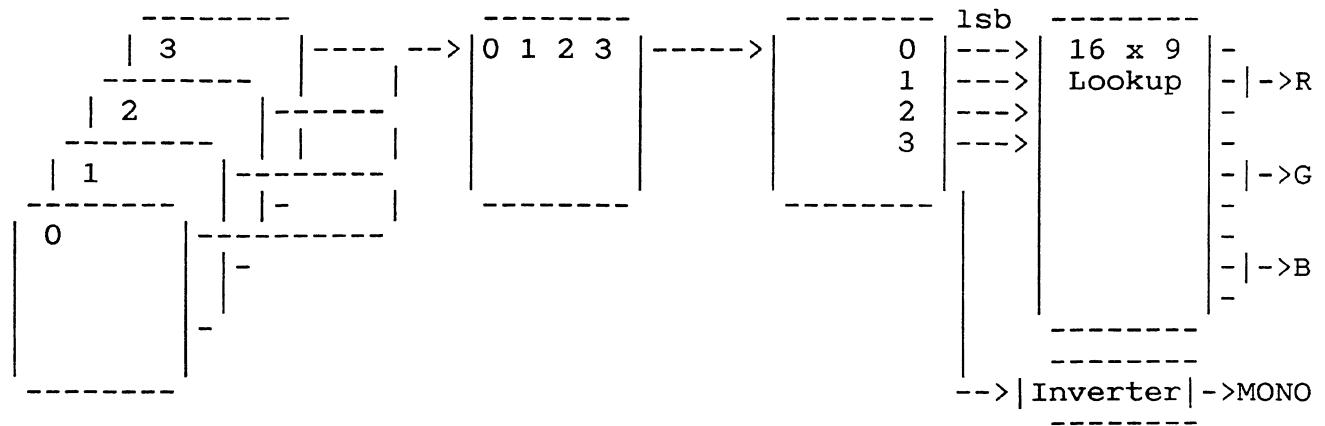
```
        --------                    --------             -------- lsb  --------
       |  3     |---- -->|0 1 2 3 |------>|        0 |--->| 16 x 9 |-
        --------  |      |        |       |        1 |--->| Lookup |-|->R
      |  2     |--|---   |        |       |        2 |--->|        |-
       --------  | |  |  |        |       |        3 |--->|        |-
    |  1     |---|-|-----|        |       |          |              -|->G
     --------  | | |-  | |        |        --------             -
  |  0     |---|-|----- -  --------                 |           -|->B
   |        |  | |-                                 |           -
  |        |   | -                                  |            --------
  |        |    -                                   |            --------
  |        |                                         -->|Inverter|->MONO
   --------                                              --------
```

Logical BitMap   Video Display   Video Shift   Color Palette
Planes   Memory   Register   and 3 Bit
                                                                DACs

4. Music Subsystem

```
 ----------                      ----------
|          |                    |Music     |
|          |                    |Subsystem |
 ----------                      ----------
     |              ----------        |
 --------|          |--------|
          |          |
           ----------
               |
                    ----------
            --------|          |
                   |          |
                    ----------
```
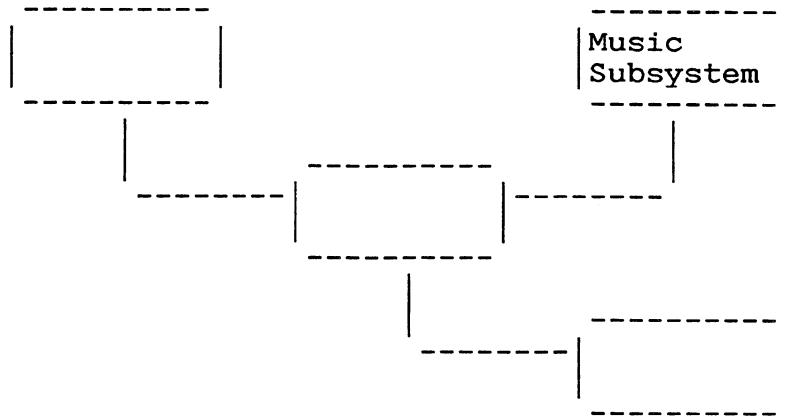
The ST music subsystem is composed of a programmable sound synthesizer and a musical instrument serial interface. The interface provides high speed serial communication of musical data to and from more sophisticated synthesizer device subsystems.

4.1. Sound Synthesizer

The YM-2149 Programmable Sound Generator produces music synthesis, sound effects, and audio feedback (eg alarms and key clicks). With an applied clock input of 2 MHz, the PSG is capable of providing a frequency response range between 30 Hz (audible) and 125 KHz (post-audible). The generator places a minimal amount of processing burden on the main system (which acts as the sequencer) and has the ability to perform using three independent voice channels. The three sound channel outputs are mixed, along with Audio In, and sent to an external television or monitor speaker (the PSG has built in digital to analog converters).

The sound generator's internal registers are accessed via the PSG Register Select Register (write only, reset: registers all zeros). The tone generator registers control a basic square wave while the noise generator register controls a frequency modulated square wave of pseudo random pulse width. Tones and noise can be mixed over individual channels by using the mixer control register. The amplitude registers allow the specification of a fixed amplitude or of a variable amplitude when used with the envelope generator. The envelope generator registers permit the entry of a skewed attack-decay-sustain-release envelope in the form of a continue-attack-alternate-hold envelope.

4.2. Musical Instrument Communications

The Musical Instrument Digital Interface (MIDI) allows
the integration of the ST with music synthesizers, sequenc-
ers, drum boxes, and other devices possessing MIDI inter-
faces. High speed (31.25 Kbaud) serial communication of
keyboard and program information is provided by two ports,
MIDI OUT and MIDI IN (MIDI OUT also supports the optional
MIDI THRU port).

The MIDI bus permits up to 16 channels in one of three
network addressing modes: Omni (all units addressed simul-
taneously, power up default), Poly (each unit addressed
separately), and Mono (each unit voice addressed
separately). Information is communicated via five types of
data format (data bytes, most significant bit: status 1,
data 0) which are prioritized from highest to lowest as:
System Reset (default conditions, should not be sent on
power up to avoid deadlock), System Exclusive (manufacturer
unique data: Sequential Circuits, Kawai, Roland, Korg,
Yamaha), System Real Time (synchronization), System Common
(broadcast), and Channel (note selections, program data,
etc).

5. Device Subsystems

```
   ----------              ----------
  |          |            |          |
   ----------              ----------
       |                        |
       |      ----------        |
   --------  |          | -------
            |          |
             ----------
                 |
                 |          ----------
          --------|Device    |
                  |Subsystems|
                   ----------
```
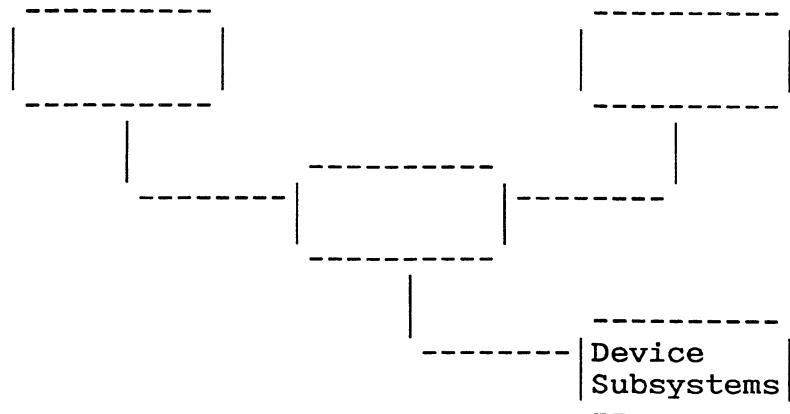
The ST supports seven device subsystems: an intelli-
gent keyboard, video interface, parallel interface, RS232
interface, MIDI interface, floppy disk interface, and hard
disk interface. Included with each device interface
description is a port pin assignment chart with the ST and
programmable signals justified left (pins that are not con-
nected are not shown). The connector type on the ST is
shown above each pin list with an S designating a female
socket and a P designating a male plug.

5.1. Intelligent Keyboard

The Atari Intelligent Keyboard (ikbd) transmits encoded
make/break key scan codes (with two key rollover),
mouse/trackball data, joystick data, and time of day.   The
ikbd receives commands as well, with bidirectional communi-
cation controlled on the ST side by an MC6850 Asynchronous
Communications Interface Adapter supplied with transmit and
receive clock inputs of 500 KHz. The data transfer rate is
a constant 7812.5 bits/sec which can be generated by setting
the ACIA Counter Divide Select to divide by 64.   All ikbd
functions such as key scanning, mouse tracking, command
parsing, etc. are performed by a 1 MHz HD6301V1 8 bit Micro-
computer Unit.

The ikbd is equipped with a combination mouse/joystick
port and a joystick only port. The Atari Two Button Mouse
is a mechanical, opto-mechanical, or optical mouse with the
following minimal performance characteristics: a resolution
of 100 counts/inch (4 counts/mm), a maximum velocity of 10
inches/second (250 mm/second), and a maximum pulse phase
error of 50 percent. The Atari Joystick is a 4 direction

switch-type joystick with one fire button. The ikbd can
report movement using one of three mouse/joystick modes:
mouse with joystick, disabled mouse with joystick, and joys-
tick with joystick.

----- Mouse/Joystick0 Port Pin Assignments ---------------

```
       ST            DB 9P
                     ----                                   ----
IKBD MATRIX           1  |<--- XB Pulse / Up Switch --------|
IKBD MATRIX           2  |<--- XA Pulse / Down Switch ------|
IKBD MATRIX           3  |<--- YA Pulse / Left Switch ------|
IKBD MATRIX           4  |<--- YB Pulse / Right Switch -----|
IKBD MCU              6  |<--- Left Button / Fire Button ---|
                      7  |---- Power --------------------->  |
                      8  |---- Ground ----------------------|
IKBD MCU              9  |<--- Right Button / Joy1 Fire ----|
                     ----                                   ----
```


Signal Characteristics

```
        mouse pins 1-4          TTL levels.
        joystick0 pins 1-4      TTL levels.
        pin 6                   TTL levels, closure to ground.
        pin 7                   +5 VDC.
        pin 9                   TTL levels, closure to ground.
```


Mouse Phase Directions

```
            POSITIVE RIGHT (UP)            NEGATIVE LEFT (DOWN)

         .    _____        _____               _____        _____
XA (YA)  |   |     |  |   |     |  |       |  |     |  |   |     |  |
         . --     _____        _____       _____        _____       --

         .    _____        _____               _____        _____
XB (YB)  |   |     |  |   |     |  |       |  |     |  |   |     |  |
         . -----     _____         --       --       _____         -----
```
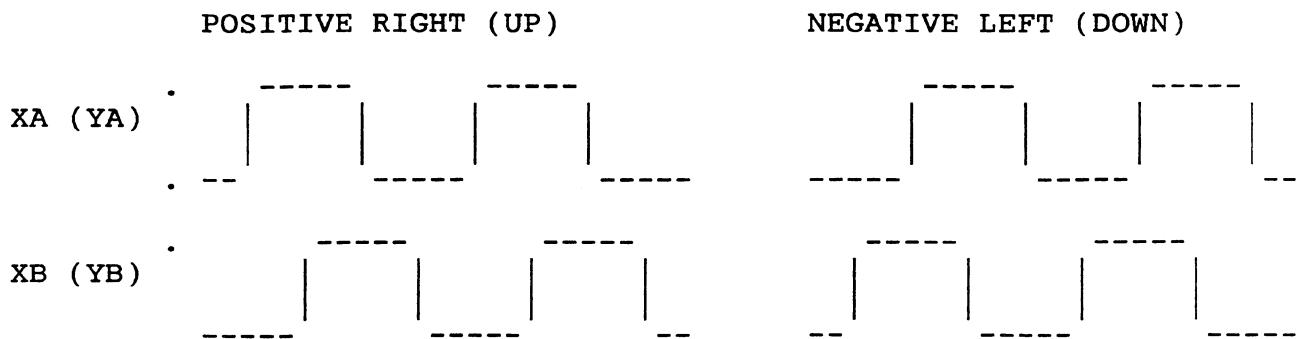
```
----- Joystick1 Port Pin Assignments ---------------

     ST              DB 9P
                     ----                              ----
IKBD MATRIX           1   |<--- Up Switch --------------------|
IKBD MATRIX           2   |<--- Down Switch ----------------|
IKBD MATRIX           3   |<--- Left Switch ----------------|
IKBD MATRIX           4   |<--- Right Switch ---------------|
IKBD MCU              6   |<--- Fire Button ----------------|
                      7   |---- Power --------------------->|
                      8   |---- Ground ---------------------|
                     ----                              ----
```

Signal Characteristics

> pins 1-4,6   TTL levels.
> pin 7   +5 VDC.

5.2. Video Interface

The ST video display interface supports low resolution (320 x 200 or 640 x 200) television receivers and composite monitors, low resolution (320 x 200 or 640 x 200) RGB monitors, and medium resolution (640 x 400) monochrome monitors. Both NTSC and PAL color encoding standards are available in two separate configurations of the video interface hardware. For United States television receivers, the modulated RF display signal is provided on two adjacent broadcast channels: channel 2 (55.25 MHz) and channel 3 (61.25 MHz). In order to protect against monitor damage while in medium resolution monochrome mode, the Monochrome Monitor Detect signal is provided as an interrupt on the MK68901 Multi Function Peripheral and can be tested to determine the presence of a monochrome monitor (active low, any change will generate the interrupt if enabled).

External/Internal syncs and 50/60 Hz field rates are selected via the Sync Mode Register (read/write, reset: all zeros). The YM-2149 Programmable Sound Generator I/O Port A provides a General Purpose Output for use in the control of functions such as the remote selection of monitor external or internal sync. Two autovector interrupts are generated to allow software synchronization with horizontal and vertical blanking intervals. The Horizontal Blanking (down) Counter MFP Timer B has an active high input signal and produces an interrupt when the counter times out (Event Count Mode). The horizontal blanking counter actually uses display enable, the first of which occurs at the end of the

first display line. The video display shift mode should be
selected during the vertical blanking interval.

----- Video Port Pin Assignments ---------------

    Television
    ST   RCA Pin Jack
                    ----   ----
              core |---- RF Modulated Video --------->|
            shield |---- Ground ----------------------|
                    ----   ----
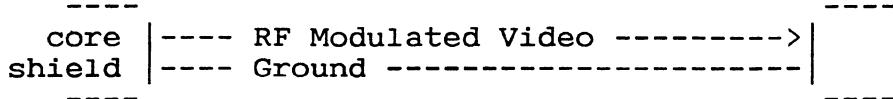
    Monitor
    ST   Circular DIN 13S
                    ----   ----
              1 |---- Audio Out ------------------->|
              2 |---- Composite Video ------------->|
PSG I/O A   3 |---- General Purpose Output ----->|
MFP   4 |<--- Monochrome Detect -----------|
              5 |<--- Audio In --------------------|
              6 |---- Green ----------------------->|
              7 |---- Red ------------------------->|
              8 |---- Peritel Power -------------->|
              9 |---- Horizontal Sync ------------>|
             10 |---- Blue ------------------------>|
             11 |---- Monochrome ----------------->|
             12 |---- Vertical Sync -------------->|
             13 |---- Ground ----------------------|
                    ----   ----
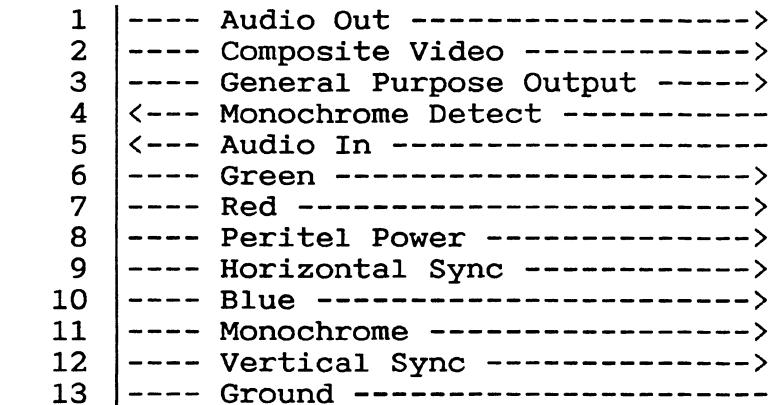
Signal Characteristics

        pin 1   1 VDC peak to peak, 10 Kohm.
        pin 2   1 VDC peak to peak, 75 ohm.
        pin 3   TTL levels, assertion not assigned.
        pin 4   TTL levels, active low,
                                1 Kohm pullup resistor to +5 VDC.
        pin 5   1 VDC peak to peak, 10 Kohm.
        pins 6-7   1 VDC peak to peak, 75 ohm.
        pin 8   +12 VDC pullup.
        pin 9   5 VDC active low, 3.3 Kohm.
        pin 10   1 VDC peak to peak, 75 ohm.
        pin 11   1 VDC peak to peak, 75 ohm.
        pin 12   5 VDC active low, 3.3 Kohm.

5.3. Parallel Interface

The ST parallel interface supports Centronics STROBE from the YM-2149 PSG for data synchronization and Centronics BUSY to the MK68901 MFP (ACKNLG is not supported) for handshaking. Eight bits of read/write data are handled through I/O Port B on the PSG at a typical data transfer rate of 4000 bytes/second.

----- Parallel Port Pin Assignments ---------------

```
      ST                DB 25S
                         ----                                    ----
PSG I/O A            1  |---- Centronics STROBE ---------->|
PSG I/O B            2  |<--- Data 0 --------------------->|
PSG I/O B            3  |<--- Data 1 --------------------->|
PSG I/O B            4  |<--- Data 2 --------------------->|
PSG I/O B            5  |<--- Data 3 --------------------->|
PSG I/O B            6  |<--- Data 4 --------------------->|
PSG I/O B            7  |<--- Data 5 --------------------->|
PSG I/O B            8  |<--- Data 6 --------------------->|
PSG I/O B            9  |<--- Data 7 --------------------->|
MFP                 11  |<--- Centronics BUSY -------------|
                 18-25  |---- Ground ----------------------|
                         ----                                    ----
```


Signal Characteristics

```
        pin 1                TTL levels, active low.
        pins 2-9             TTL levels.
        pin 11               TTL levels, active high,
                             1 Kohm pullup resistor to +5 VDC.
```


5.4. RS 232 Interface

The ST RS232 interface provides voltage level synchronous or asynchronous serial communication. Five EIA RS232C handshake control signals are supported: Request To Send and Data Terminal Ready are transmitted through the YM-2149 PSG I/O Port A while Clear To Send, Data Carrier Detect, and Ring Indicator are received through the MK68901 MFP. The MFP USART transmit and receive clock inputs are controlled by the Baud Rate Generator MFP Timer D which is supplied with 2.4576 MHz and can support asynchronous data transfer rates from 50 to 19200 baud. One byte transmit and receive data buffers are managed by the MFP USART, which provides monitoring of buffer conditions and communication errors.

```
----- RS232 Port Pin Assignments ---------------

        ST                 DB 25P
                           ----                                    ----
                           1  |---- Protective Ground -----------|
MFP                        2  |---- Transmitted Data ----------->|
MFP                        3  |<--- Received Data ---------------|
PSG I/O A                  4  |---- Request To Send ------------>|
MFP                        5  |<--- Clear To Send ---------------|
                           7  |---- Signal Ground ---------------|
MFP                        8  |<--- Data Carrier Detect ---------|
PSG I/O A                  20 |---- Data Terminal Ready -------->|
MFP                        22 |<--- Ring Indicator --------------|
                           ----                                    ----
```

Signal Characteristics

        pins 2-5   RS232C levels.
        pins 8,20,22   RS232C levels.

5.5. MIDI Interface

The ST MIDI interface provides current loop asynchro-
nous serial communication controlled by an MC6850 ACIA sup-
plied with transmit and receive clock inputs of 500 KHz.
The data transfer rate is a constant 31.25 Kbaud which can
be generated by setting the ACIA Counter Divide Select to
divide by 16. The MIDI specification calls for serial data
to consist of eight data bits preceded by a start bit and
followed by one stop bit.

```
----- MIDI Port Pin Assignments ----------------

      MIDI OUT/THRU
      ST                  Circular DIN 5S
                          ----                        ----
MIDI IN              1  |---- THRU Transmit Data ---------->|
                     2  |---- Shield Ground ---------------|
                     3  |<--- THRU Loop Return -----------|
MIDI ACIA            4  |---- OUT Transmit Data ---------->|
                     5  |<--- OUT Loop Return ------------|
                          ----                        ----


      MIDI IN
      ST                  Circular DIN 5S
                          ----                        ----
MIDI ACIA            4  |<--- IN Receive Data -------------|
                     5  |---- IN Loop Return ------------->|
                          ----                        ----
```

Signal Characteristics

       current loop   5 ma, zero is current on.

5.6. Disk Drive Interface

    The ST floppy disk drive interface is provided through
the DMA controller to an on board WD1772 Floppy Disk Con-
troller. A total of two daisy chained floppy disk drives
(drive 0 or 1) can be supported. Commands are sent to the
FDC by first writing to the DMA Mode Control Register to
select the FDC internal command register and then writing
the desired one byte command to the Disk Controller Regis-
ter. The entire floppy disk DMA read or write sequence is
as follows:

o   select floppy drive 0 or 1 (PSG I/O Port A).
o   select floppy side 0 or 1 (PSG I/O Port A).
o   load DMA Base Address and Counter Register.
o   toggle Write/_Read to clear status (DMA Mode Control Register).
o   select DMA read or write (DMA Mode Control Register).
o   select DMA Sector Count Register (DMA Mode Control Register).
o   load DMA Sector Count Register (DMA operation trigger).
o   select FDC internal command register (DMA Mode Control Register).
o   issue FDC read or write command (Disk Controller Register).
o   DMA active until sector count is zero (DMA Status Register,
    do not poll during DMA active).
o   issue FDC force interrupt command on multi-sector transfers

except at track boundaries (Disk Controller Register).
o   check DMA error status (DMA Status Register, nondestructive).

        The detection of floppy disk removal is not supported
in hardware.

        The ST hard disk drive interface is also provided
through the DMA controller, however the Atari Hard Disk Con-
troller is off board and is sent commands using an ANSI
X3T9.2 SCSI-like (Small Computer Systems Interface) command
descriptor block protocol. The Atari Hard Disk Interface
(AHDI) supports a minimal subset of SCSI commands (Class 0
OpCodes), which are dispatched using the following fixed six
byte Atari Computer System Interface (ACSI) command packet
format:

----- ACSI Command Descriptor Block ---------------

        Byte 0 |xxxxxxxx|
                  || |||||||
                  || | -------- Operation Code
                  ----------- Controller Number
        Byte 1 |xxxxxxxx|
                  || ||||||
                  |||--------- Block Address High
                  ----------- Device Number
        Byte 2 |xxxxxxxx|
                  ||||||||
                  ----------- Block Address Mid
        Byte 3 |xxxxxxxx|
                  ||||||||
                  ----------- Block Address Low
        Byte 4 |xxxxxxxx|
                  ||||||||
                  ----------- Block Count
        Byte 5 |xxxxxxxx|
                  ||||||||
                  ----------- Control Byte
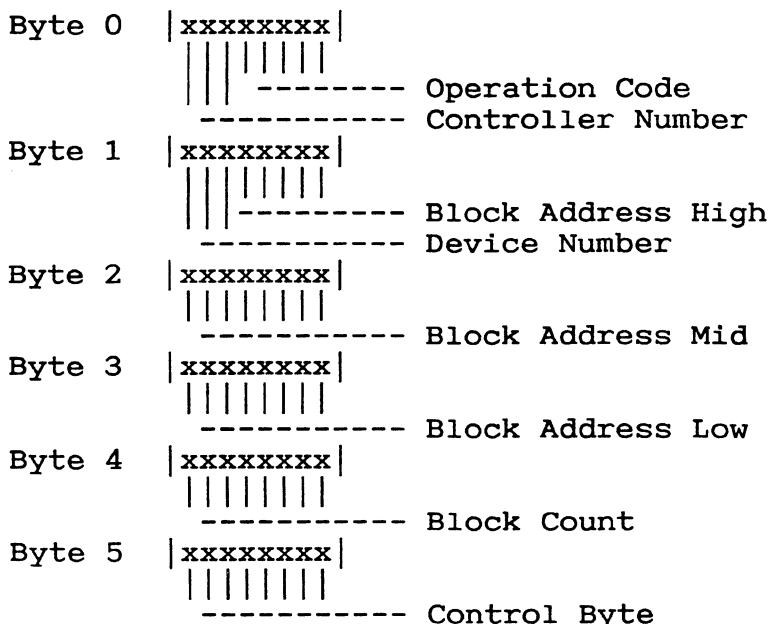
        The following is a summary of available command
OpCodes:

----- AHDI Command Summary Table ---------------

OpCode	Command
0x00	Test Unit Ready
0x05	Verify Track	*
0x06	Format Track	*
0x08	Read	*
0x0a	Write	*
0x0b	Seek
0x0d	Correction Pattern
0x15	Mode Select
0x1a	Mode Sense

        *   multisector transfer with implied seek

NOTE: subject to change.

        Commands are issued to the Atari HDC in a manner simi-
lar to that of the FDC, with the major difference being the
handshaking of a multi-byte command descriptor block.   The
entire hard disk DMA read or write sequence is as follows:

o   load DMA Base Address and Counter Register.
o   toggle Write/_Read to clear status (DMA Mode Control Register).
o   select DMA read or write (DMA Mode Control Register).
o   select DMA Sector Count Register (DMA Mode Control Register).
o   load DMA Sector Count Register (DMA operation trigger).
o   select HDC internal command register (DMA Mode Control Register).
o   issue controller select byte while clearing A0.
o   set A0 for remaining command bytes.
o   after last command byte select controller (DMA Mode Control
    Register).
o   DMA active until sector count is zero (DMA Status Register,
    do not poll during DMA active).
o   check DMA error status (DMA Status Register, nondestructive).
o   check HDC status byte and if necessary perform ECC correction
    following a Verify Track or Read Sector command.

        The format of both floppy and hard disks contain 512
byte data sectors.

----- Floppy Disk Port Pin Assignments ---------------

```
       ST                  Circular DIN 14S
       ----                ----                              ----
                           1  |<--- Read Data -------------------|
PSG I/O A                  2  |---- Side0 Select --------------->|
                           3  |---- Logic Ground ---------------|
                           4  |<--- Index Pulse ----------------|
PSG I/O A                  5  |---- Drive0 Select ------------->|
PSG I/O A                  6  |---- Drive1 Select ------------->|
                           7  |---- Logic Ground ---------------|
                           8  |---- Motor On ------------------>|
                           9  |---- Direction In -------------->|
                          10  |---- Step ---------------------->|
                          11  |---- Write Data ---------------->|
                          12  |---- Write Gate ---------------->|
                          13  |<--- Track 00 -------------------|
                          14  |<--- Write Protect --------------|
       ----                ----                              ----
```

NOTE: shield ground must not be connected on the ST side,
        the cable must have Read Data and Write Data paired
        with Logic Grounds.

Signal Characteristics

```
            pin 1                   TTL levels, active low,
                                    1 Kohm pullup resistor to +5 VDC.
            pin 2                   TTL levels, active high,
                                    high at system reset.
            pin 4                   TTL levels, active low,
                                    1 Kohm pullup resistor to +5 VDC.
            pins 5-6                TTL levels, active low,
                                    high at system reset.
            pins 8-12               TTL levels, active low (inverted).
            pins 13-14              TTL levels, active low,
                                    1 Kohm pullup resistors to +5 VDC.
```

```
----- Hard Disk Port Pin Assignments ---------------

    ST              DB 19S
                    ----                                        ----
                      1 |<--- Data 0 --------------------->|
                      2 |<--- Data 1 --------------------->|
                      3 |<--- Data 2 --------------------->|
                      4 |<--- Data 3 --------------------->|
                      5 |<--- Data 4 --------------------->|
                      6 |<--- Data 5 --------------------->|
                      7 |<--- Data 6 --------------------->|
                      8 |<--- Data 7 --------------------->|
                      9 |---- Chip Select ---------------->|
    MFP              10 |<--- Interrupt Request -----------|
                     11 |---- Ground ----------------------|
                     12 |---- Reset --------------------->|
                     13 |---- Ground ----------------------|
                     14 |---- Acknowledge --------------->|
                     15 |---- Ground ----------------------|
                     16 |---- A1 ------------------------->|
                     17 |---- Ground ----------------------|
                     18 |---- Read/Write ---------------->|
                     19 |<--- Data Request ---------------|
                    ----                                        ----
```

Signal Characteristics

```
        pins 1-8            TTL levels.
        pin 9              TTL levels, active low.
        pin 10             TTL levels, active low,
                           1 Kohm pullup resistor to +5 VDC.
        pin 12             TTL levels, active low,
                           system reset.
        pin 14             TTL levels, active low.
        pins 16,18         TTL levels.
        pin 19             TTL levels, active low,
                           1 Kohm pullup resistor to +5 VDC.
```

6. Components

     The standard configurations of the Atari ST main system, graphics subsystem, music subsystem, and device subsystems are made up of the following major hardware components:

Main

- o 8 MHz MC68000 Microprocessor Unit
- o MK68901 Multi Function Peripheral
- o 192 Kbyte ROM
- o 512 Kbyte or 1 Mbyte RAM
- o Memory Controller Chip
- o Control Logic Chip
- o DMA Controller Chip

Graphics

- o 32 Kbyte Display Memory (from main RAM)
- o Video Shift Register Chip

Music

- o YM-2149 Programmable Sound Generator

Device

- o Atari Intelligent Keyboard (ikbd)
  1 MHz HD6301V1 Microcomputer Unit
- o Atari Two Button Mouse
- o 2 MC6850 Asynchronous Communications Interface Adapters
- o WD1772 Floppy Disk Controller

7. Expansion

The Atari ST can be expanded by cartridge ROM only
which can contain a maximum of 128 Kbyte. The disclosure of
cartridge presence or memory size is not supported in
hardware. The ROM cartridge slot has the following pin
assignments (only the lower 15 address lines are available):

----- ROM Port Pin Assignments ---------------

```
    ST                 40S
                       ----                                    ----
                    1  |---- Power +5 VDC --------------->|
                    2  |---- Power +5 VDC --------------->|
                    3  |<--- Data 14 ---------------------|
                    4  |<--- Data 15 ---------------------|
                    5  |<--- Data 12 ---------------------|
                    6  |<--- Data 13 ---------------------|
                    7  |<--- Data 10 ---------------------|
                    8  |<--- Data 11 ---------------------|
                    9  |<--- Data 8 ----------------------|
                   10  |<--- Data 9 ----------------------|
                   11  |<--- Data 6 ----------------------|
                   12  |<--- Data 7 ----------------------|
                   13  |<--- Data 4 ----------------------|
                   14  |<--- Data 5 ----------------------|
                   15  |<--- Data 2 ----------------------|
                   16  |<--- Data 3 ----------------------|
                   17  |<--- Data 0 ----------------------|
                   18  |<--- Data 1 ----------------------|
                   19  |---- Address 13 ----------------->|
                   20  |---- Address 15 ----------------->|
                   21  |---- Address 8 ------------------>|
                   22  |---- Address 14 ----------------->|
                   23  |---- Address 7 ------------------>|
                   24  |---- Address 9 ------------------>|
                   25  |---- Address 6 ------------------>|
                   26  |---- Address 10 ----------------->|
                   27  |---- Address 5 ------------------>|
                   28  |---- Address 12 ----------------->|
                   29  |---- Address 11 ----------------->|
                   30  |---- Address 4 ------------------>|
                   31  |---- ROM3 Select ---------------->|
                   32  |---- Address 3 ------------------>|
                   33  |---- ROM4 Select ---------------->|
                   34  |---- Address 2 ------------------>|
                   35  |---- _Upper Data Strobe --------->|
                   36  |---- Address 1 ------------------>|
                   37  |---- _Lower Data Strobe --------->|
                38-40  |---- Ground ----------------------|
                       ----                                    ----
```

8. Memory Map

     The first 2 Kbyte of ST memory is reserved for the
exception vector table and supervisor stack. This area
along with I/O space is protected for supervisor references
only.   Accessing supervisor protected areas while in the
user state will result in a bus error. A 4 word portion of
ROM is shadowed at the start of RAM for the reset stack
pointer and program counter. Writing to this area or any
ROM location will also result in a bus error. The following
is a map of ST memory:

----- ST Memory Map ---------------

```
                  ----------------
00 0000   | ROM            |    Reset:Supervisor Stack Pointer
00 0004   | ROM            |    Reset:Program Counter
00 0008   | RAM            |    0 Kbyte RAM
                  ----------------
                        .
                  ----------------
08 0000   | RAM            |    512 Kbyte RAM
                  ----------------
                        .
                  ----------------
10 0000   | RAM            |    1 Mbyte RAM
                  ----------------
                        .
                        .
                        .
                  ----------------
fa 0000   | ROM            |    320 Kbyte ROM
                  ----------------
                        .
                  ----------------
fc 0000   | ROM            |    Reset:Supervisor Stack Pointer
fc 0004   | ROM            |    Reset:Program Counter
fc 0008   | ROM            |    192 Kbyte ROM
fe ffff   | ROM            |    0 Kbyte ROM
                  ----------------
                        .
                        .
                        .
                  ----------------
ff 8000   | I/O            |    Configuration Registers
ff 8200   | I/O            |    Display Registers
ff 8400   | I/O            |    Reserved
ff 8600   | I/O            |    DMA/Disk Registers
ff 8800   | I/O            |    Sound Registers
                  ----------------
                        .
                  ----------------
ff fa00   | I/O            |    MC68xxx Registers
ff fc00   | I/O            |    MC68xx Registers
                  ----------------
```

9. I/O Map

The ST I/O space ranges from ff 0000 to ff ffff, with MC68000 and MC6800 peripheral internal registers starting at ff fa00 and ff fc00 respectively. Accessing reserved I/O addresses will result in a bus error. Bit values for various read and/or write registers are labeled as active One/_Zero (always mask out unused field bits). The following is a map of ST I/O space:

Configuration

```
ff 8001   R/W           |----xxxx|     Memory Configuration
                            ||||
                          -------     Bank0         Bank1 (not used)
                          0000        128 Kbyte     128 Kbyte
                          0001        128 Kbyte     512 Kbyte
                          0010        128 Kbyte       2 Mbyte
                          0011        Reserved
                          0100        512 Kbyte     128 Kbyte
                          0101        512 Kbyte     512 Kbyte
                          0110        512 Kbyte       2 Mbyte
                          0111        Reserved
                          1000          2 Mbyte     128 Kbyte
                          1001          2 Mbyte     512 Kbyte
                          1010          2 Mbyte       2 Mbyte
                          1011        Reserved
                          11xx        Reserved
```

Display

```
ff 8201   R/W           |xxxxxxxx|     Video Base High
ff 8203   R/W           |xxxxxxxx|     Video Base Mid

ff 8205   R             |xxxxxxxx|     Video Address Counter High
ff 8207   R             |xxxxxxxx|     Video Address Counter Mid
ff 8209   R             |xxxxxxxx|     Video Address Counter Low

ff 820a   R/W           |------xx|     Sync Mode
                              ||
                              | ----    External/_Internal Sync
                               -----    50 Hz/_60 Hz Field Rate

ff 8240   R/W           |-----xxx-xxx-xxx|     Palette Color 0/0 (Border)
                              ||| ||| |||
                              ||| ||| || ----     Inverted/_Normal Monochrome
                              ||| ||| |||
                              ||| ||| ------     Blue
                              ||| ----------     Green
                               ------------     Red
ff 8242   R/W           |-----xxx-xxx-xxx|     Palette Color 1/1
```

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```
ff 8244    R/W    |-----xxx-xxx-xxx|    Palette Color 2/2
ff 8246    R/W    |-----xxx-xxx-xxx|    Palette Color 3/3
ff 8248    R/W    |-----xxx-xxx-xxx|    Palette Color 4
ff 824a    R/W    |-----xxx-xxx-xxx|    Palette Color 5
ff 824c    R/W    |-----xxx-xxx-xxx|    Palette Color 6
ff 824e    R/W    |-----xxx-xxx-xxx|    Palette Color 7
ff 8250    R/W    |-----xxx-xxx-xxx|    Palette Color 8
ff 8252    R/W    |-----xxx-xxx-xxx|    Palette Color 9
ff 8254    R/W    |-----xxx-xxx-xxx|    Palette Color 10
ff 8256    R/W    |-----xxx-xxx-xxx|    Palette Color 11
ff 8258    R/W    |-----xxx-xxx-xxx|    Palette Color 12
ff 825a    R/W    |-----xxx-xxx-xxx|    Palette Color 13
ff 825c    R/W    |-----xxx-xxx-xxx|    Palette Color 14
ff 825e    R/W .  |-----xxx-xxx-xxx|    Palette Color 15


ff 8260    R/W              |------xx|    Shift Mode
                                  ||
                            00            320 x 200, 4 Plane
                            01            640 x 200, 2 Plane
                            10            640 x 400, 1 Plane
                            11            Reserved
```

RESERVED
‾‾‾‾‾‾‾‾

```
ff 8400           |----------------|    Reserved
```

DMA/Disk
‾‾‾‾‾‾‾‾

```
ff 8600           |----------------|    Reserved
ff 8602           |----------------|    Reserved

ff 8604    R/W    |--------xxxxxxxx|    Disk Controller (Word Access)

ff 8606    R      |-------------xxx|    DMA Status (Word Access)
                                |||
                                || ----   _Error Status
                                | -----   ‾Sector Count Zero Status
                                 ------   ‾Data Request Inact Status
ff 8606    W      |--------xxxxxxxx-|    DMA Mode Control (Word Access)
                          ||||||||
                          |||||||| -----   A0
                          ||||||| ------   A1
                          ||||||  -------   HDC/_FDC Register Select
                          |||||  --------   Sector Count Registr Select
                          ||||0            Reserved
                          ||| ----------   Disable/_Enable DMA
                          || -----------   FDC/_HDC
                           ------------   Write/_Read

ff 8609    R/W    |xxxxxxxx|    DMA Base and Counter High
ff 860b    R/W    |xxxxxxxx|    DMA Base and Counter Mid
```

```
ff 860d   R/W            |xxxxxxxx|   DMA Base and Counter Low
```

Sound

```
ff 8800   R              |xxxxxxxx|   PSG Read Data
                          ||||||||      I/O Port B
                          --------------  Parallel Interface Data
ff 8800   W              |xxxxxxxx|   PSG Register Select
                            ||||
                            -------      Register Number
                   0000              Channel A Fine Tune
                   0001              Channel A Coarse Tune
                   0010              Channel B Fine Tune
                   0011              Channel B Coarse Tune
                   0100              Channel C Fine Tune
                   0101              Channel C Coarse Tune
                   0110              Noise Generator Control
                   0111              Mixer Control - I/O Enable
                   1000              Channel A Amplitude
                   1001              Channel B Amplitude
                   1010              Channel C Amplitude
                   1011              Envelope Period Fine Tune
                   1100              Envelope Period Coarse Tune
                   1101              I/O Port A (Output Only)
                   1111              I/O Port B

ff 8802   W              |xxxxxxxx|   PSG Write Data
                                         I/O Port A
                                 -------     Flppy Sde0/_Side1 Select
                                 -------     Floppy _Drive0 Select
                                 --------    Floppy _Drive1 Select
                                 ---------   RS232 Request To Send
                                 ----------  RS232 Data Termnal Ready
                                 ----------- Centronics _STROBE
                                 ------------ General Purpose Output
                          -------------- Reserved
                          ||||||||      I/O Port B
                          -------------- Parallel Interface Data
```

MC68xxx

```
ff fa01            |xxxxxxxx|   MFP General Purpose I/O
ff fa03            |xxxxxxxx|   MFP Active Edge
ff fa05            |xxxxxxxx|   MFP Data Direction
ff fa07            |xxxxxxxx|   MFP Interrupt Enable A
ff fa09            |xxxxxxxx|   MFP Interrupt Enable B
ff fa0b            |xxxxxxxx|   MFP Interrupt Pending A
ff fa0d            |xxxxxxxx|   MFP Interrupt Pending B
ff fa0f            |xxxxxxxx|   MFP Interrupt In-Service A
ff fa11            |xxxxxxxx|   MFP Interrupt In-Service B
ff fa13            |xxxxxxxx|   MFP Interrupt Mask A
```

```
ff fa15                    |xxxxxxxx|   MFP Interrupt Mask B
ff fa17                    |xxxxxxxx|   MFP Vector
ff fa19                    |xxxxxxxx|   MFP Timer A Control
ff fa1b                    |xxxxxxxx|   MFP Timer B Control
ff fa1d                    |xxxxxxxx|   MFP Timers C and D Control
ff fa1f                    |xxxxxxxx|   MFP Timer A Data
ff fa21                    |xxxxxxxx|   MFP Timer B Data
ff fa23                    |xxxxxxxx|   MFP Timer C Data
ff fa25                    |xxxxxxxx|   MFP Timer D Data
ff fa27                    |xxxxxxxx|   MFP Sync Character
ff fa29                    |xxxxxxxx|   MFP USART Control
ff fa2b                    |xxxxxxxx|   MFP Receiver Status
ff fa2d                    |xxxxxxxx|   MFP Transmitter Status
ff fa2f                    |xxxxxxxx|   MFP USART Data
```

MC68xx

```
ff fc00                    |xxxxxxxx|   Keyboard ACIA Control
ff fc02                    |xxxxxxxx|   Keyboard ACIA Data

ff fc04                    |xxxxxxxx|   MIDI ACIA Control
ff fc06                    |xxxxxxxx|   MIDI ACIA Data
```

10. Interrupt Table

    The following tables list the ST interrupt and signal
priority assignments:

----- MC68000 Interrupt Autovector ---------------

```
 ----------------   -----------------------------------
| Level            | Definition                        |
 ----------------   -----------------------------------
| 7 (HIGHEST)      | NMI                               |
| 6                | MK68901 MFP                       |
| 5                |                                   |
| 4                | Vertical Blanking (Sync)          |
| 3                |                                   |
| 2                | Horizontal Blanking (Sync)        |
| 1 (LOWEST)       |                                   |
 ----------------   -----------------------------------
```

NOTE: only interrupt priority level inputs 1 and 2 are used.

----- MK68901 Interrupt Control ---------------

```
 ----------------   -----------------------------------
| Priority         | Definition                        |
 ----------------   -----------------------------------
| 15 (HIGHEST)     | Monochrome Monitor Detect      I7 |
| 14               | RS232 Ring Indicator           I6 |
| 13               | System Clock / BUSY            TA |
| 12               | RS232 Receive Buffer Full         |
| 11               | RS232 Receive Error               |
| 10               | RS232 Transmit Buffer Empty       |
|  9               | RS232 Transmit Error              |
|  8               | Horizontal Blanking Counter    TB |
|  7               | Disk Drive Controller          I5 |
|  6               | Keyboard and MIDI              I4 |
|  5               | Timer C                        TC |
|  4               | RS232 Baud Rate Generator      TD |
|  3               | GPU Operation Done             I3 |
|  2               | RS232 Clear To Send            I2 |
|  1               | RS232 Data Carrier Detect      I1 |
|  0 (LOWEST)      | Centronics BUSY                I0 |
 ----------------   -----------------------------------
```

NOTE: the MC6850 ACIA Interrupt Request status bit must be tested
        to differentiate between keyboard and MIDI interrupts.

11. Case Design

     The ST is primarily designed as a keyboard computer
with external video display, disk drives, and power supply.
The top panel contains the keyboard, ventilation slots (bot-
tom also), and power on LED. The side panels contain the
expansion ROM slot and mouse/joystick ports. The back panel
contains the on/off switch, reset button, channel select
switch, power connector, and all remaining device connec-
tors: video, parallel, RS232, MIDI, and disk drive inter-
faces.

     The device ports are labeled with International Elec-
trotechnical Commission-like symbols in combinations of pic-
tograms and phonetic transcriptions (captions). In the case
of MIDI, the specification explicitly requires that the MIDI
connectors be labeled MIDI OUT, MIDI IN, and MIDI THRU (if
applicable).

12. Power Supply

An external DC power supply provides power to the main
system board, keyboard, expansion ROM, and expansion RAM.
All power levels are regulated for over-voltage and over-
current protection. The following are minimal power supply
specifications:

AC Input   115 VAC 10% at 60 Hz (fused)

DC Output   +5 VDC at 3 A 5%
                            +12 VDC at .03 A 10%
                            -12 VDC at .03 A 10%

----- Power Port Pin Assignments ---------------

```
     ST              DIN 7P
                     ----                                ----
                  1 |<--- +5 VDC ----------------------|
                  3 |---- Ground ----------------------|
                  4 |<--- +12 VDC ---------------------|
                  5 |<--- -12 VDC ---------------------|
                  6 |<--- +5 VDC ----------------------|
                  7 |---- Ground ----------------------|
                     ----                                ----
```
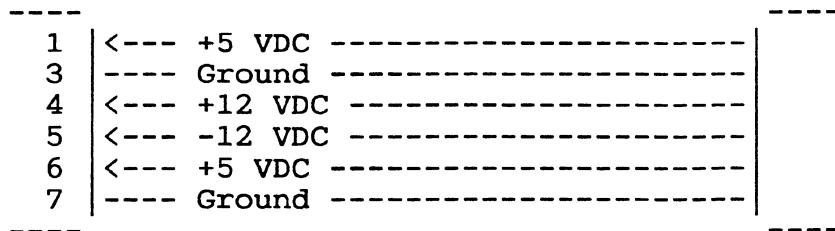
Appendix A -- ikbd Keyboard Layout

     The surface of the Atari Intelligent Keyboard is formed
from four   distinct   ergonomic   units: a QWERTY typewriter
matrix, a function key array, a screen control cluster,   and
a calculator numeric keypad. As a whole, the United States
version of the keyboard layout is DEC VT100-like with the
exception of the following items:

o   removed keys -- [break], [line feed], [no scroll], [set up].

o   repositioned keys -- [caps lock], cursor control keys,
    programmable function keys.

o   added keys -- [alternate], [help], [undo], [insert], [clear/home],
    10 programmable function keys.

o   improvements -- DEC VT200-style inverted T cursor control
    keys, full calculator function numeric keypad.

     Please note that the left [shift] key is intentionally
large to allow space for an extra ISO required key (see ISO
2530-1975).   Atari ikbd International Layouts will   be
designed for the following countries:

o   United Kingdom
o   United States
o   Finland
o   Norway / Denmark
o   Sweden
o   Japan
o   Germany
o   French Canada
o   France
o   Italy
o   Spain

NOTE: the 'HELP' and 'UNDO' keys will be left untranslated.

Appendix B -- References

General

A Hitchhiker's Guide to the BIOS

Digital Research GEM Software Documentation

Main System

Motorola MC68000 16-Bit Microprocessor User's Manual, Fourth Edition

Mostek MK68901 Multi Function Peripheral Data Sheet

Graphics Subsystem

Adele Goldberg and David Robson, 'Smalltalk-80: The Language and Its Implementation', Addison-Wesley, Reading Massachusetts, 1983, Chapter 18.

Music Subsystem

General Instrument AY-3-8910 Programmable Sound Generator Data Sheet

MIDI Musical Instrument Digital Interface Specification 1.0

Device Subsystems

Atari Intelligent Keyboard (ikbd) Protocol and Specification

Motorola MC6850 Asynchronous Communications Interface Adapter Data Sheet

Centronics Parallel Interface Specification

Electronic Industries Association RS232C Standard

Western Digital WD1770/1772 Floppy Disk Controller Data Sheet

Specification of the Atari Computer System Interface (ACSI)

Specification of the Atari Hard Disk Interface (AHDI)

Appendix C -- Notes

General

851125A   An address error occurs when a word instruction is
           used on a byte address.

Main System

841017B   The DMA Base Address and Counter Register must be
           loaded in low, mid, high order.

Graphics Subsystem

841017C   None.

Music Subsystem

841017D   The YM-2149 PSG I/O space and registers should be
           set up as critical regions in software.

Device Subsystems

841017F   Poll or service the Disk Drive Controller inter-
           rupt on the MK68901 MFP General Purpose I/O Regis-
           ter to detect the completion of a WD1772 FDC com-
           mand.   Do   not   poll   the   FDC Busy or DMA Sector
           Count Zero status bits.

841017G   Select the Sector Count Register before testing
           the DMA Status Register Error bit.

841017H   Do not set the 30 ms Settling Delay bit on WD1772
           FDC type 2 and 3 command executions.

841017I   A force interrupt should be issued after a few
           seconds (ie time out) on all commands sent to the
           WD1772 FDC.

841017J   Wait until the WD1772 FDC Motor On status is low
           before deselecting a floppy drive.

841017K   A floppy disk drive configuration table should be
           maintained in software to accommodate a diverse
           selection of 3.5 inch floppy disk drives.   Two
           floppy disk drives currently under evaluation have
           the following characteristics:
           o 500 Kbyte unformatted, 80 cylinders, one head,
           3 ms stepping rate.
           o 1 Mbyte unformatted, 80 cylinders, two heads, 3
           ms stepping rate.

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